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# Reduced hardware costs with software and hardware implementation of digital methods multistage discrete Fourier transform on programmable logic devices

## Снижение аппаратных затрат при программно-аппаратной реализации цифровых методов многоступенчатого дискретного преобразования Фурье на программируемых логических интегральных схемах

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**Abstract**

Let us consider questions, which are connected to the research of terms of hardware and software implementation digital signal processing (DSP) methods. Theoretical basis of this research are methods of non-recursive difference of digital filtration with integer difference coefficients different orders of difference and methods of multistage discrete Fourier transform (DFT) based on such digital filtration. The purpose of the study is the research and formalization of necessary and sufficient condition of lowering hardware costs in hardware and software implementation of methods multistage DFT of digital signals on programmable logic devices (PLD). For reaching the research goal there are used methods of direct search and comparative analysis of results of such realization of methods of multi-stage DFT of digital multi-band signals, while filtering these signals, which are based on their non-recursive difference digital filtering with integer difference values coefficients and different orders of magnitude of difference. There are described abilities and specialties of PLD, which are built using architecture of a coarse-grained or fine-grained architecture or using combined architecture, which connects the

**Аннотация**

Рассмотрены вопросы, связанные с исследованием условий программно-аппаратной реализации цифровых методов обработки сигналов. Теоретической основой этого исследования стали методы нерекурсивной разностной цифровой фильтрации с целочисленными разностными коэффициентами различных порядков разности и методы многоступенчатого дискретного преобразования Фурье на основе такой цифровой фильтрации. Цель исследования - определение и формализация необходимого и достаточного условия снижения аппаратных затрат при программно-аппаратной реализации методов многоступенчатого дискретного преобразования Фурье цифровых сигналов на программируемых логических интегральных схемах. Для достижения цели исследования использованы методы направленного перебора и сравнительного анализа результатов такой реализации методов многоступенчатого дискретного преобразования Фурье цифровых сигналов многополосной фильтрацией этих сигналов на основе их нерекурсивной

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convenience of implementing digital processing algorithms signals on the basis of tables of code conversion and reconfigurable memory modules. It is clear that a necessary and sufficient condition of lowering hardware costs in terms of hardware and software realization of methods for multi-stage DFT of digital signals on PLD is the triviality of meanings of integer difference coefficients of a non-recursive difference digital high difference orders' filtration, which ensure this information. There is mentioned a formula, which allows making such condition. The practical significance of the research results consists of defining the necessary and sufficient condition of lowering hardware costs in terms of hardware and software implementation on PLD methods of multi-stage DFT signals based on their non-recursive digital difference filtering with integer values differential coefficients of various orders of magnitude difference. The novelty of research results lies in formalization of this condition. The reliability of the research results confirms their compliance with the results of well-known developments of DSP methods.

**Keywords:** differential digital filter, DSP, DFT, multi-band filtering, PLD.

разностной цифровой фильтрации с целочисленными разностными коэффициентами и различных порядков разности. Описаны возможности и особенности программируемых логических интегральных схем, построенных по крупномодульной архитектуре или по мелкомодульной архитектуре, или по комбинированной архитектуре, сочетающей удобство реализации алгоритмов цифровой обработки сигналов на базе таблиц перекодировок и реконфигурируемых модулей памяти. Определено, что необходимым и достаточным условием снижения аппаратных затрат при программно-аппаратной реализации методов многоступенчатого дискретного преобразования Фурье цифровых сигналов на программируемых логических интегральных схемах является тривиальность значений целочисленных разностных коэффициентов нерекурсивной разностной цифровой фильтрации высоких порядков разности, обеспечивающей это преобразование. Приведена формула, позволяющая выполнять такое условие. Практическая значимость результатов исследования состоит в определении необходимого и достаточного условия снижения аппаратных затрат при программно-аппаратной реализации на программируемых логических интегральных схемах методов многоступенчатого дискретного преобразования Фурье цифровых сигналов на основе их нерекурсивной разностной цифровой фильтрации с целочисленными разностными коэффициентами различных порядков разности. Новизна результатов исследования заключается в формализации этого условия. Достоверность результатов исследования подтверждается их соответствием результатам известных разработок цифровых методов обработки сигналов.

**Ключевые слова:** дискретное преобразование Фурье, многополосная фильтрация, программируемые логические интегральные схемы, разностный цифровой фильтр, цифровая обработка сигналов.

## Introduction

Accidents and catastrophes of medium- and long-haul aircrafts in the end of 2019 and the beginning of 2020, which happened as result of damage or partial malfunction of aviation engines made the problem of automatic control of work quality engines of airliners during takeoff and climb actual (Burova, 2017; Burova, 2019). One of the possible ways of solving this problem can be an automatic assessment of levels of parasitic vibrations of aircraft engines in flight by digital methods of DFT (Zalmanzon, 1989).

Such methods of digital procession of signals (DPS) are realized on digital signal processors (DSP) or on PLD (Vityazev, 2017; Vityazev, V. V., Vityazev, S. V., 2007; Speransky, 1997; Speransky, 2008; Steshenko, 2000; Steshenko, 2007). However, the inequality of speeds of completing the arithmetic operations multiplication and addition in their hardware and software implementation on PLD set up the necessity of lowering the amount of hardware-based algorithmic multiplication operations in DFT algorithms with PLD-realization (Kaplun, Merkucheva, 2009; Shcherbakov, Steshenko, Gubanov, 2000; Shinakov, Burov, 1998; Shinakov, Burov, 2000; Shinakov, Burov, Burova, 2000; Burov, Burova, 2010; Burova, 2020; Burova, Kabakov, 2020).

The purpose of the study is to define and formalize the necessary and sufficient conditions reducing hardware costs for hardware and software implementation of digital methods multi-stage DFT (MDFT) on a PLD.

**Theoretical basis**

Theoretical basis of lowering the hardware costs in hardware and software realization of methods MDFT of digital signal *x(n*T)* should be considered digital methods calculation of grades *y(l, n*T)* coefficients of *L*-point DFT of such signal by its *L*-band filtration *K-th* order by different digital filters *K+M* order with $k_M$ different coefficients of *M-th* order $h_p(l,M,k_M,)$ using formula (1) with $k_M$=0,1,2… *K+M*-1, *l*=1,2,3… *L*, *m*=1,2,3… *M*, *n*=0,1,2… *N*-1 and *L*≤*N* (Kuzkin, 1983; Shinakov, Burov, 1998; Shinakov, Burov, 2000; Shinakov, Burov, Burova, 2000; Burov, Burova, 2000; Burov, Burova, 2010; Burova 2020):

$$y(l, n\cdot T) = \sum_{k=0}^{K+M-1} \sum_{k_0=0}^{k} \sum_{k_1=0}^{k_0} \ldots \sum_{k_m=0}^{k_{m-1}} \ldots \sum_{k_{M-1}=0}^{k_{M-2}} \sum_{k_M=0}^{k_{M-1}} h_{\text{p}}(l, M, k_M) \cdot x(n\cdot T - k_M \cdot T). \quad (1)$$

**Methodology**

The study used the methods of comparative analysis of the MDF results of digital signals by their multi-band filtering by difference digital filters with different integer difference coefficients of different orders of difference (Burova, 2020; Burova, Kabakov, 2020). As the research materials, we used PLD built on large-module architecture and small-module architecture, as well as a combined architecture that combines the convenience of implementing DSP algorithms based on conversion tables and reconfigurable memory modules (Kanashchenkov, Matveev, Novikov, 2018).

**Research results**

**Abilities and specialties of PLD**

In comparison to usual digital microchips, logic of PLD work is not defined while making, but set through programming. For PLD programming there are used specialized programmers and debugging environments that allow setting the desired structure of a digital device in the form of a circuit diagram or program on special languages of describing microelectronic equipment.

Nowadays programmers and producers of microelectronic equipment DSP more often try to use exactly PLD, what is defined by a big number of hardware interfaces in comparison to DSP, and by flexibility while wiring boards, which allow submitting to the chip data of arbitrary capacity. Besides, the cost of PLD is lower than the cost of DSP, while the conditions of their exploitation are the same.

The functionality of PLD depends on the amount of DSP elementary devices, which are placed on it. Every device, which is placed there, uses a defined quantity of its resources. One of the most critical elements in PLD is multipliers. Moreover, the composition of each PLD includes a fixed number of multipliers that can be used to build a certain number of systems, or one complex scheme. Minimization of realized on PLD hardware multipliers allows optimizing the usage of PLD resources, which means freeing some space on it for other devices, lowering this way, taken volume of hardware means and lowering material costs on hardware realization of digital algorithms of DFT. Some producers of PLD suggest program processors for their PLD, which can be modified for a special task, and then built in PLD. This way the lowering of the place on a printed circuit board and simplifying the design of the PLD itself is provided, due to speed.

A common estimate of the logical capacity of PLD is the number of equivalent modules, defined as the average number of 2AND-NOT gates needed to implement an equivalent project on PLD and the base matrix crystal. Moreover, this assessment is very arbitrary, since PLD do not contain 2AND-NOT gates in their pure form. However, for conducting a comparative analysis of the hardware costs for PLD implementation of various architectures of the hardware-software implementation of DFT methods with a minimum number of arithmetic operations of multiplication and addition, such an estimate is quite suitable.

However, mathematic formalization of requirements of hardware costs on hardware and software realization of DFT methods, which is univocal while using DSP, turns out to be controversial while using PLD. This is due to multivariance of possible scheme decisions of hardware and software realizations of DFT methods on PLD.

The main history of PLD is supposed to be counted from 1970, when the company TEXAS INSTRUMENTS designed programmable digital microchip TMS2000. Up to middle 1980s PLD was auxiliary element base for making single and small-series simple combinational and sequential automatic machines with complexity up to several tens of equivalent valves 2AND-NOT. However, in 1983 there was built the company ALTERA, in 1984 the company XILINX, in 1985 the corporation ACTEL, which became the main developers of PLD and the ideology of using PLD. Form the moment of its forming these and a row of other companies actively develop new classes and families of PLD, different in the architecture, which differ by the availability of new functions. Through time, there is a clearly manifesting tendency of specialization of PLD market, when this or that company becomes a leader on one of the PLD areas of development.

The easiest and developed before architectures of PLD are architectures SPLD and CPLD with high level of elements' integration on the crystal. The functionality of such PLD encodes in non-volatile memory that is why there is no necessity of their reprogramming while their turning on. However, this PLD are used only in interface schemes, because they do not allow realization hard algorithms of DSP. For realization of such algorithms there are used PLD, built on FPGA architecture. They have elements that are more logical and more flexible architecture, than PLD, built using SPLD and CPLD architectures.

However, in PLD realizations of computational algorithms of digital DFT methods, regardless of the architecture of the used FPGA, the equality of the speed of arithmetic operations of multiplication and addition is achieved mainly due to hardware costs.

**PLD, built on FPGA architecture**

PLD, built on FPGA architecture, consist of logical blocks and commuting paths. Logical blocks of these PLD, in their turn, consist of one or some simple logical elements. Due to a big amount of logical elements, PLD comes out to be a convenient tool for hardware and software realization of the DSP algorithms, the main operations in which are the operations of multiplication, addition and delay of the signal.

There are two main classes of FPGA architecture: coarse-grained and fine-grained. Coarse-grained architecture of FPGA class consists of big logical blocks, which can contain some tables of transcoding and programmable intra-unit connections. Fine-grained architecture of FPGA class consists of a big amount of rather simple logical blocks. The advantage of coarse-grained technology is productivity, and fine-grained structure is characterized by big flexibility while synthesis and working in more complicated structures. Both classes of FPGA architecture have been developed before and are successfully implemented in PLD.

PLD FPGA, regardless to the class of their architecture, contain multiplication-summation blocks and logic elements, as a rule, based on tables of transcoding, and commuting blocks, which are programmable connection matrixes. The program for PLD FPGA is situated in distributed memory. If it is made on the basis of volatile cells of statistic operative memorable device, the program is not saved in case of power failure of the microcircuit. In this case, during every turning on of microcircuit power it is necessary to re-configure it, using bootloader, which can be built in PLD FPGA. If the distributed memory is made on the basis of volatile cells of Flash memory or jumpers ANTIFUSE, the program is saved in case of power failure.

Further development of FPGA architecture was the two-level architecture of the connection matrix, characterized for the PLD family FLEX10K. Logical elements inside logical blocks are connected using

local programmable connection matrix, which allows connecting any elements. Logic blocks are connected among themselves and with input-output elements through a global programmable matrix of connections. Moreover, the local and global matrixes of compounds have a continuous structure, in which a continuous channel is allocated for each connection.

However, despite the development of FPGA architecture, the equality of speeds of arithmetic operations of multiplication and addition in hardware and software realization of DFT methods even on perspective PLD FPGA is reached mainly due to the usage of hardware tools.

**PLD of the company ALTERA**

Company ALTERA is one of the technologic leaders, constantly developing advanced and perspective production in PLD sphere. New PLD family, made by this company on the basis of microarchitecture, gives a new level of processing power and productivity. With the growth of the bit depth of the data representation at this level, the dimension of elementary multipliers and adders in the PLD increases and a larger number of logical elements are required for the PLD implementation of complex DSP algorithms. That is why in the recent years sharply increased the logical capacity of PLD, which are produced by the company ALTERA through FPGA technology. Now they can have millions of equivalent valves 2AND-NOT on one crystal.

The development of PLD technology the company ALTERA leads using the path of combining architectures, which consist of convenience of DSP algorithms realization, based on tables of transcoding and re-configuring memory modules, characterized exactly for FPGA PLD architecture. This allows using the perspective PLD family APEX20K of the company ALTERA as the basic element base for hardware realization of the idea “system-on-the-crystal”, whose basis is the maximization of the integration level of the electronic DSP system in one crystal. The components of “system-on-the-crystal” are developed separately and are kept as files of parameterizable modules. The final structure of microchip is made on the basis of these “virtual components”, which are also called “intellectual property units” using EDA electronic design systems software. Moreover, in PLD of the company ALTERA there is the ability of programming in this system directly on the board of microchip, which of course lowers the cost of PLD technology ownership.

Thanks to standardization, in “system-on-the-crystal” it is possible to combine “virtual components” from different developers and use ready modules of mega functions of different functional units, which are made especially for solution of hard DSP decisions. For example, mega functions, which realize the standard DFT algorithms and digital filtration. The development of ready-made mega functions by the efforts of third companies is proceeding rapidly. That is why the company ALTERA created the support program for developers partners of mega functions for PLD, which is called ALTERA MEGAFUNCTION PARTNERS PROGRAM, which includes dozens of mega function independent developer firms.

Due to the peculiarities of its architecture, modern and promising PLD from ALTERA allow achieving the best performance indicators in comparison with other methods of software and hardware implementation of DSP algorithms. However, in software and hardware implementations of DFT methods, even on ALTERA PLD, the equality of the speed of arithmetic operations of multiplication and addition is achieved mainly by hardware.

**Necessary and sufficient condition for reducing hardware costs in PLD implementation of digital MDFT methods**

According to the results of the study, necessary and sufficient condition for reducing hardware costs in the software and hardware implementation of digital MDFT methods of digital signal $x(n*T)$ through its multi-band filtering by difference digital filters, the duality of the integer difference coefficients of these filters can and should be considered $h_p(l,M,k_M)$, which provides a digital convolution $h_p(l, M, k_M)*x(n*T-k_M*T)$ only by summing the time samples of this signal according to formula (2) without performing multiplication operations when $k_M$=0,1,2…$K$+$M$-1, $l$=1,2,3…$L$, $n$=0,1,2…$N$-1 and $L \leq N$:

$$h_p(l,M,k_M)\cdot x(n\cdot T-k_M\cdot T)=\begin{cases} x(n\cdot T-k_M\cdot T)+x(n\cdot T-k_M\cdot T)+ \\ \quad +x(n\cdot T-k_M\cdot T)+x(n\cdot T-k_M\cdot T) \text{ if } h_p(l,M,k_M)=2^2; \\ x(n\cdot T-k_M\cdot T)+x(n\cdot T-k_M\cdot T) \text{ if } h_p(l,M,k_M)=2^1; \\ x(n\cdot T-k_M\cdot T) \text{ if } h_p(l,M,k_M)=2^0; \\ -x(n\cdot T-k_M\cdot T) \text{ if } h_p(l,M,k_M)=-2^0; \\ -x(n\cdot T-k_M\cdot T)-x(n\cdot T-k_M\cdot T) \text{ if } h_p(l,M,k_M)=-2^1; \\ -x(n\cdot T-k_M\cdot T)-x(n\cdot T-k_M\cdot T)- \\ \quad -x(n\cdot T-k_M\cdot T)-x(n\cdot T-k_M\cdot T) \text{ if } h_p(l,M,k_M)=-2^2. \end{cases} \quad (2)$$

**Discussion**

The idea of lowering the amount of arithmetic multiplication operations in digital DFT algorithms are due to the usage of hardware tools for reaching the equality of speeds of performing arithmetic operations of multiplication and addition on PLD.

The usage of methods of differential digital filtration, while building digital DFT algorithms allows fully exclude arithmetic multiplication operations from these algorithms, with duality of difference coefficients of such filtering.

The usage of PLD, due to the specialties of their architecture, demands a lower volume of hardware tools for hardware and software realization of digital MDFT algorithms than the usage of DSP.

The practical significance of the study is to determine the conditions for reducing hardware costs in the software and hardware implementation of digital algorithms MDFT on PLD.

The novelty of the proposed research results lies in the formalization of the conditions for minimizing hardware costs in the hardware-software implementation of digital algorithms MDFT on PLD.

However, for the successful usage of methods of difference digital filtering with binary difference coefficients in the software and hardware implementation of digital MDPF algorithms, it is desirable to develop methods for the synthesis of difference digital filters with binary difference coefficients of high orders of difference.

**Conclusion**

The suggested formalization of necessary and sufficient condition of lowering hardware costs in terms of hardware and software realization of digital MDFT methods on PLD will allow minimizing such costs through a complete rejection of algorithmic operations of multiplication in MDFT algorithms. The usage of this condition on practice will provide completing MDFT digital signals on PLD only by addition and shift operations.

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