# Artículo de investigación <br> Digital signal processing without performing arithmetic multiplication operations 

Цифровая обработка сигналов без выполнения арифметических операций умножения

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#### Abstract

Issues related to the frequency selection of digital signals by the methods of their transversal difference digital filtering and multistage discrete Fourier transform with a minimum number of arithmetic multiplication operations are considered. The concept of deductive processing of digital signals is defined, which does not require arithmetic operations of multiplication. There are basic formulas for this processing of digital signals by recursive methods of difference filtering and multistage Fourier transform, which allow replacing the performance of arithmetic multiplication operations by the performance of addition operations.


Keywords: Digital signal, digital signal processing, discrete Fourier transform, programmable logic device, transversal difference digital filtering.


#### Abstract

Аннотация Рассмотрены вопросы, связанные с частотной селекцией цифровых сигналов методами их трансверсальной разностной цифровой фильтрации и многоступенчатого дискретного преобразования Фурье с минимальным числом арифметических операций умножения. Определено понятие дедуктивной обработки цифровых сигналов, не требующей выполнения арифметических операций умножения. Приведены основные формулы такой обработки цифровых сигналов рекуррентными методами разностной цифровой фильтрации и многоступенчатого преобразования Фурье, позволяющими заменять выполнение арифметических операций умножения выполнением арифметических операций сложения. Ключевые слова: дискретное преобразование Фурье, программируемая логическая интегральная схема, трансверсальная разностная цифровая фильтрация, цифровая обработка сигналов, цифровой сигнал.


## Introduction

The demand for digital spectral analysis algorithms stimulated the development of filtering and discrete Fourier transform methods of digital signals for their frequency selection with the minimum possible number of multiplication operations (Kuzkin, 1983; Vityazev, 1993; Shinakov, Burov, 1998; Shinakov, Burov, 2000; Burov, Burova, 2000; Shinakov, Burov, Burova, 2000; Shcherbakov, Steshenko, Gubanov, 2000; Kaplun, 2007; Kaplun, 2009; Burov, Burova, 2010).

Gradual improvement of the elementary base of electronic computer engineering periodically updates the development of digital signal processing methods with the minimum possible number of multiplication

[^0]operations required for its implementation (Burov, Burova, 2010; Burova, 2019). These methods were relevant in the realization of digital signal processing algorithms both on integrated circuits of the first series of microprocessor sets, and on programmable logic devices (Steshenko, 2000; Shcherbakov, Steshenko, Gubanov, 2000; Steshenko, 2007; Kaplun, 2007; Kaplun, 2009). The use of digital signal processors and coprocessors of multiplication made possible to equalize the speed of arithmetic operations of multiplication and addition during its operation (Speransky, 1997; Speransky, 2008; Vityazev, Vityazev, 2007; Vityazev, Zaitsev, Vityazev, 2008). However, the creation of programmable logic devices and elementary nanoelectronic devices was looking for the development of digital signal processing methods without performing arithmetic multiplication operations (Steshenko, 2000; Steshenko, 2007; Schuka, 2007). These methods can be developed and should be developed on the basis of the methods of deductive processing of digital signals (Burov, Burova, 2010).

The purpose of the research is to find a solution to the problem of digital signal processing without arithmetic multiplication operations.

When developing digital algorithms for this signal processing, the computational procedures of finite difference methods and the Coordinate Rotation Digital Computer method were used (CORDIC) (Shinakov, Burov, 2000; Burov, Burova, 2010). It allowed reducing hardware costs for the frequency selection of digital signals during their deductive processing (Vityazev, 1993; Burov, Burova, 2010).

Theoretical basis, methods, and algorithms of deductive processing of digital signals were proposed and described in the works of some authors (Kuzkin, 1983; Shinakov, Burov, 1998; Shinakov, Burov, 2000; Shinakov, Burov, Burova, 2000; Burov, Burova, 2000; Burov, Burova, 2010).

However, the transfer of digital computer engineering to the nanoelectronic elementary base makes the development of the theory, methods and algorithms of deductive processing of digital signals still relevant and in demand (Schuka, 2007). The novelty of deductive processing of digital signals is the combined use of the recurrent representation of digital signals and the recurrent conversion of them without performing arithmetic multiplication operations with special processor implementation of digital signal processing algorithms.

## Theoretical basis

Deductive processing of digital signals is provided by the methods of transversal difference digital filtering and multistage discrete Fourier transform of signals without performing arithmetic multiplication operations (Kuzkin, 1983; Shinakov, Burov, 1998; Shinakov, Burov, 2000; Shinakov, Burov, Burova, 2000). This processing of digital signals consists of their recurrent representation and conversion by finite difference methods, transversal difference digital filtering and multistage discrete Fourier transform in implementing processing algorithms of these signals on programmable logic devices or elementary nanoelectronic devices in which the equality of the rates of multiplication and addition is achieved by hardware.

Deductive processing of digital signals is a combination of digital methods of their processing, which ensure its implementation without performing arithmetic multiplication operations (Schuka, 2007).

## Methodology

Research materials are time counts of polyharmonic digital signals.
Research methods are the methods of transversal difference digital filtering and multistage discrete Fourier transform of signals that do not require arithmetic multiplication operations (Kuzkin, 1983; Shinakov, Burov, 1998; Shinakov, Burov, 2000; Shinakov, Burov, Burova, 2000; Burov, Burova, 2000; Burov, Burova, 2010).

## Results

The gain-frequency parameters of these digital signals $\left\{x_{0}(n \cdot T)\right\}$ with sampling periods $T, n=0,1,2 \ldots N-1$, such as parasitic vibrations of aircraft engines, sonar target noise or echo signals during echoencephaloscopy, gradually change in time at a given interval [ $0, T_{x}$ ) if $T_{x}>N \cdot T$. Time sample available
for digital processing $\left\{x_{0}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$ of the signal that changes in time, can be a sequence of counts $\left\{x_{1}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$ with the «first-order increments» $\left\{\Delta x_{1}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$. Each of its counts is the arithmetic sum of the previous one and its «first-order increment» $\Delta x_{1}(n \cdot T)$, which is calculated by the finite difference method according to the following formula (1):
$x_{1}(n \cdot T)=x_{1}(n \cdot T-T)+\Delta x_{1}(n \cdot T), n=1,2,3 \ldots N-1, x_{1}(0)=x_{0}(0)$.
This increment is defined as the difference between the values of the current and previous counts of the original sample by the following formula (2):
$\Delta x_{1}(n \cdot T)=x_{0}(n \cdot T)-x_{0}(n \cdot T-T), n=1,2,3 \ldots N-1, \Delta x_{1}(0)=x_{1}(0)$.
We replaced this sequence $\left\{x_{1}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$ with the sample of «first-order increments», which requires less memory to store its elements. Any time count of the initial sample $\left\{x_{0}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$ should be calculated on the basis of «first-order increments» $\left\{\Delta x_{1}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$ during the digital signal processing. But $\left\{\Delta x_{1}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$ can also be arithmetic sums. Therefore, we should represent each successive «first-order increment» by the sum of the previous one and its «second-order increment» $\Delta x_{2}(n \cdot T)$, calculated by the finite difference method by the following formula (3):
$\Delta x_{2}(n \cdot T)=\Delta x_{1}(n \cdot T)-\Delta x_{1}(n \cdot T-T), n=1,2,3 \ldots N-1, \Delta x_{2}(0)=\Delta x_{1}(0)$.
Then we replaced the sample $\left\{\Delta x_{1}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$ with a sample of «second-order increment» $\left\{\Delta x_{2}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$. Increasing the order of differences we will get more low-discharge $<l$-order increments» $\left\{\Delta x_{l}(n \cdot T)\right\}, l=1,2,3 \ldots L, n=0,1,2 \ldots N-1$, up to binary $(+2,+1,0,-1,-2)$, trivial $(+1,0,-1)$ or single $(+1,-1)$ by the formula (4), according to the formulas (1), (2) and (3):
$x_{0}(n \cdot T)=\sum_{n_{0}=0}^{n} \sum_{n_{1}=0}^{n_{0}} \ldots \sum_{n_{l}=0}^{n_{l-1}} \ldots \sum_{n_{L-1}=0}^{n_{L-2}} \sum_{n_{L}=0}^{n_{L-1}} \Delta x_{L}\left(n_{L} \cdot T\right), n=0,1,2 \ldots N-1, l=1,2,3 \ldots L$.
Digital processing of a combination of «l-order increments» $\left\{\Delta x_{l}(n \cdot T)\right\}, l=1,2,3 \ldots L, n=0,1,2 \ldots N-1$ using the methods of transversal difference digital filtering and multistage discrete Fourier transform on the basis of transversal difference digital filtering does not require multiplication operations. This digital processing of a signal is deductive processing of digital signals. During this processing the $K$-order digital filtering coefficients $\left\{h^{*}(k)\right\}, k=0,1,2 \ldots K-1$ are replaced by the binary, trivial or single difference ones of the transversal difference digital filtering of the $K+M$-order and $M$-order of the difference $\left\{h_{\mathrm{p}}\left(M, k_{M}\right)\right\}$, $k_{M}=0,1,2 \ldots K+M-1$ by the following formula (5):
$h^{*}(k)=\sum_{k_{0}=0}^{k} \sum_{k_{1}=0}^{k_{0}} \ldots \sum_{k_{m}=0}^{k_{m-1}} \ldots \sum_{k_{M-1}=0}^{k_{M-2}} \sum_{k_{M}=0}^{k_{M-1}} h_{\mathrm{p}}\left(M, k_{M}\right), m=1,2,3 \ldots M$.
Figure 1 shows the graphs of the formation of the coefficients $\left\{h^{*}(k)\right\}, k=0,1,2 \ldots K-1$, K-order digital filtering that is equivalent to the transversal difference digital filtering of the $(K+M)$-order and $M$-order of the difference with $k_{M}$ integer trivial difference coefficients $\left\{h_{\mathrm{p}}\left(M, k_{M}\right)\right\}, k_{M}=0,1,2 \ldots K+M-1$ and the construction of the impulse response $\left\{h^{*}(k)\right\}, k=0,1,2 \ldots K-1$, the equivalent digital filter of the $K$-order in the form $(\operatorname{Sin}[x] / x)$, which is indicated by a bold dashed line, where $M=0,1,2 \ldots 3$ (Shinakov, Burov, 1998; Shinakov, Burov, Burova, 2000).


Figure 1. Graphs of the formation of the coefficients $\left\{h^{*}(k)\right\}, k=0,1,2 \ldots K-1$ and construction of impulse response $\left\{h^{*}(k)\right\}, k=0,1,2 \ldots K-1$

The multistage discrete Fourier transform is performed on the basis of multiband transversal difference digital filtering with low-discharge integer difference coefficients, which has a branched pyramidal structure.

The idea of reducing the number of arithmetic multiplication operation in digital signal processing algorithms is due to the inequality of the speed of arithmetic operations and addition in elementary devices of digital computing tools. It has been successfully implemented in the digital algorithms of the fast and discrete Fourier transform based on number-theoretic transformations. However, in modern programmable logic integrated circuits and elementary nanoelectronic devices the equality of the speeds of the multiplication and addition operations is achieved mainly due to hardware overhead.

The number of multiplication operations in digital signal processing was minimized only in a number of algorithms of fast Fourier transform with a minimum number of multiplications and Mersenne numbertheoretic transforms (Winograd algorithms). The use of transversal difference digital filtering algorithms made possible to develop a method of multistage discrete Fourier transform, which does not require arithmetic multiplication operations. The essence of this method is to divide the complex signal spectrum «step by step» into a series of bands with their spectra shifted to the low-frequency domain by the CORDIC algorithms with trivial values ( $\pm 1, \pm i$ ) of twiddle factors and low-frequency filtering of time counts at each step of the multi-stage discrete Fourier transform with transversal difference digital filters with binary ( $-2,-$ $1,0,+1,+2)$, trivial ( $-1,0,+1$ ), or single difference coefficients.

An increase in the number of addition operations and shift in multistage discrete Fourier transform algorithms provides the level of accuracy of digital signal processing, like in fast Fourier transform algorithms. However, the multistage discrete Fourier transform allows calculating only the necessary components of the spectrum of the complex signal. To calculate them with a step change in the frequency resolution of the spectrum, it is possible to use the computational resource already used before, due to the
pyramid structure of the multistage discrete Fourier transform. Even with a zero degree of parallelization of computations, the multistage discrete Fourier transform requires less computational resources for special processor implementation of digital signal processing algorithms, compared with the fast one

Deductive processing of digital signals by the methods of finite differences, transversal difference digital filtering and multistage discrete Fourier transform using formulas (4) and (5) provides the basic procedure for digital signal processing, $K$-order digital convolution $\left\{s_{K}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$ by arithmetic operations of addition and shift of low-discharge integer values of the coefficients of transversal difference digital filtering of the $K$-order and $M$-order of the difference $\left\{h_{\mathrm{p}}\left(M, k_{M}\right)\right\}, k_{M}=0,1,2 \ldots K+M-1$ and $<L$-order increments» $\left\{\Delta x_{L}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$, of the initial signal count $\left\{x_{0}(n \cdot T)\right\}, n=0,1,2 \ldots N-1$ by the following formula (6):

$$
\begin{align*}
& s_{K}(n \cdot T)=\sum_{k=0}^{K-1} h^{*}(k) \cdot x_{0}(n \cdot T-k \cdot T)= \\
& \quad=\sum_{k=0}^{K+M-1} \sum_{k_{0}=0}^{k} \sum_{k_{1}=0}^{k_{0}} \ldots \sum_{k_{M}=0}^{k_{M-1}} \sum_{n_{0}=0}^{n} \sum_{n_{1}=0}^{n_{0}} \ldots \sum_{n_{L}=0}^{n_{L-1}} h_{\mathrm{p}}\left(M, k_{M}\right) \cdot \Delta x_{L}\left(n_{L} \cdot T-k_{M} \cdot T\right) \tag{6}
\end{align*}
$$

## Discussion

Deductive processing of digital signals is in the combined application of the methods of transversal difference digital filtering with low-discharge integer coefficients and the method of multistage discrete Fourier transform based on this filtering to construct digital signal processing algorithms. This processing is the deductive processing with a zero order of differences. Deductive processing with high orders of differences minimizes the number of arithmetic multiplication operations in the designed algorithms for digital signal processing. Deductive processing of digital signals makes possible to reduce the amount of computational resource required for the special processor implementation of digital signal processing algorithms on programmable logic integrated circuits and elementary nanoelectronic devices, in which the equality of the speed of arithmetic operations of multiplication and addition is achieved by hardware.

The reliability of the proposed solution to the problem of digital signal processing without performing arithmetic multiplication operations is confirmed by the practical results of software and hardware modeling, since the results of this modeling are consistent with the frequency selection of digital signals by the methods of fast Fourier transform with a minimum number of multiplication operations and scientific and practical developments, the description of which is we can find in different scientific publications (Kuzkin, 1983; Vityazev, 1993; Shinakov, Burov, 1998; Shcherbakov, Steshenko, Gubanov, 2000; Shinakov, Burov, 2000; Shinakov, Burov, Burova, 2000; Burov, Burova, 2000; Kaplun, 2007; Kaplun, 2009; Burov, Burova, 2010).

## Conclusion

The proposed solution to the problem of digital signal processing without performing arithmetic multiplication operations allows saving the computational resource required to implement algorithms for digital signal processing on programmable logic devices or elementary nanoelectronic devices. This processing of digital signals must be carried out on the basis of the methods of transversal difference digital filtering and multistage discrete Fourier transform, in the algorithms of which the implementation of arithmetic multiplication operations is replaced by the performance of arithmetic addition operations.

The use of these methods helps to reduce the cost of implementing digital signal processing algorithms on programmable logic devices on the basis of the principle «valve-ruble».

## References

Burov Yu. Ya., Burova A.Yu (2010). Deductive processing of digital signals based on the method of finite differences and differential methods of digital filtering and multi-step discrete Fourier transform, which does not require performing arithmetic operations of multiplication. Russian Scientific and Technical Society of Radio Engineering, Electronics and Communication named after A.S. Popov: 65 Scientific
session devoted to radio day: Theses of reports. Moscow: Russian Scientific and Technical Society of Radio Engineering, Electronics and Communication, 425-428.
Burov Yu.Ya., Burova A.Yu. (2000). Synthesis of the recurrence digital filters. Russian Scientific and Technical Society of Radio Engineering, Electronics and Communication named after A. S. Popov: LV Scientific session, dedicated to Radio Day: Theses of reports. Moscow: Russian Scientific and Technical Society of Radio Engineering, Electronics and Communication, 261.
Burova A.Yu. (2019). Minimisation of asymmetry of thrust of the dual-flow turbojet engines of the airliner in accordance with the results of the system analysis of the thrust parameters. Asia Life Sciences Supplement, 21(2), 1-11.
Kaplun D.I. (2007). Non-recursive digital filters without multiplications. Information and Space. St. Petersburg: Finestreet.
Kaplun D.I. (2009). Non-recursive digital filters without multiplications. Information and Space. St. Petersburg: CJSC "Institute of Telecommunications.
Kuzkin V.S. (1983). Difference digital filtering. Radiotechnics. 1, 52-54.
Schuka A.A. (2007). Nanotranzistors in Nanoelectronics. Radiotechnics, 9, 41-47.
Shcherbakov M.A., Steshenko V.B., Gubanov D.A. (2000). Digital polynomial filtering in real time: algorithms and ways of implementation on programmable logic devices implementation. Proceedings of the Third International Conference "Digital signal processing and its application" (DSPA'2000). 1., 19-26. Shinakov Yu.S., Burov Yu.Ya (2000). Method of adaptive multistage shift and filtering of harmonic signal components. Telecommunication. 1, 15-17.
Shinakov Yu.S., Burov Yu. Ya. (1998). Difference digital filtering with integer coefficients. Proceedings of The First International Conference "Digital signal processing and its applications" (DSPA'98). 2., 94-99.
Shinakov Yu.S., Burov Yu. Ya., Burova A.Yu. (2000). Theory, methods and algorithms of difference digital filtering. Proceedings of the Third International Conference "Digital signal processing and its application" (DSPA'2000), November 29-December 1, 2000. 1., 96-99.
Speransky V.S. (1997). Digital signal processors and their application for the formation and processing of signals: a Training manual. Moscow: Technical University of Communications and Informatics.
Speransky V.S. (2008). Signal microprocessors and their application in telecommunication systems and electronics. Moscow: Hot Line.
Steshenko V.B. (2000). Programmable logic devices implementation by firm ALTERA: designing devices signal processing. Moscow: DODEKA.
Steshenko V.B. (2007). Programmable logic devices implementation by firm ALTERA: element base, design system and hardware description languages. Moscow: DODEKA.
Vityazev V.V. (1993). Digital frequency signal selection. Moscow: Radio and Communication.
Vityazev V.V., Vityazev V.V. (2007). Digital signal processors TMS320C67x by Texas Instruments. Ryazan: Ryazan State Radio Engineering University.
Vityazev V.V., Zaitsev A.A., Vityazev S.V. (2008). Multi-speed signal processing: retrospective and current state. Part 1. Digital Signal Processing, 1, 12-21.
Vityazev V.V., Zaitsev A.A., Vityazev S.V. (2008). Multi-speed signal processing: retrospective and current state. Part 1. Digital Signal Processing, 3, 2-9.


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